

System Architecture

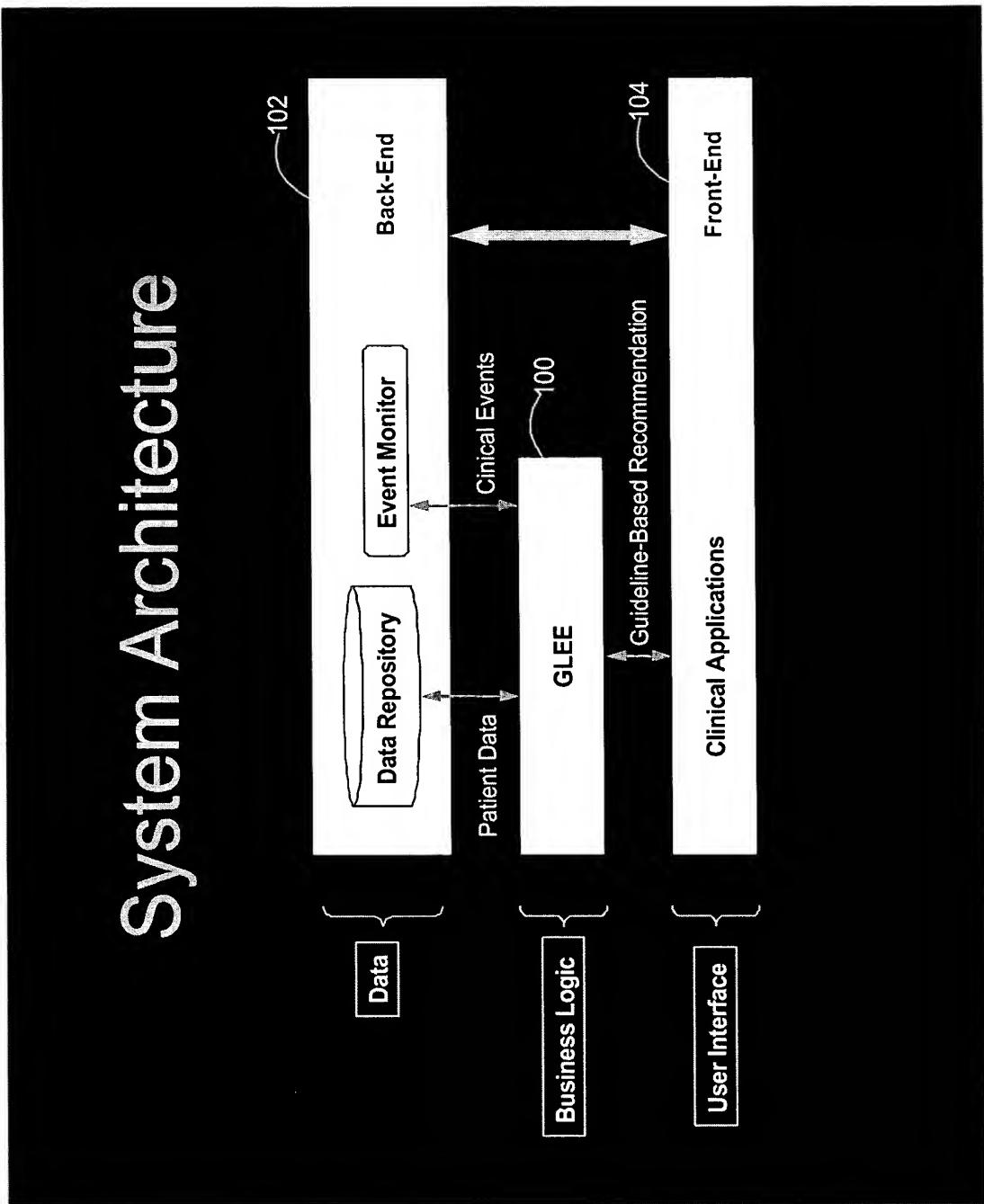


Fig. 1

Internal Structure

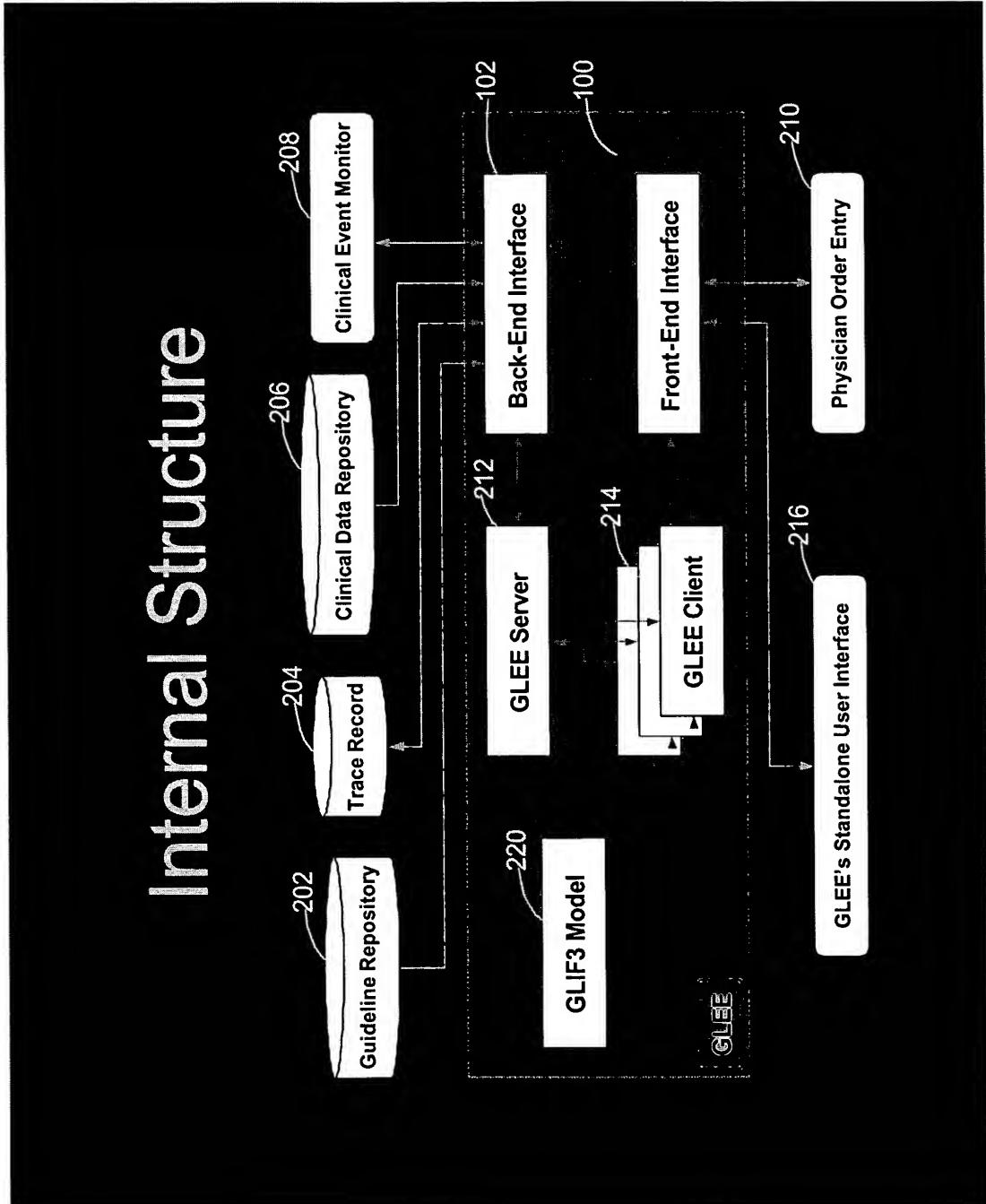


Fig. 2

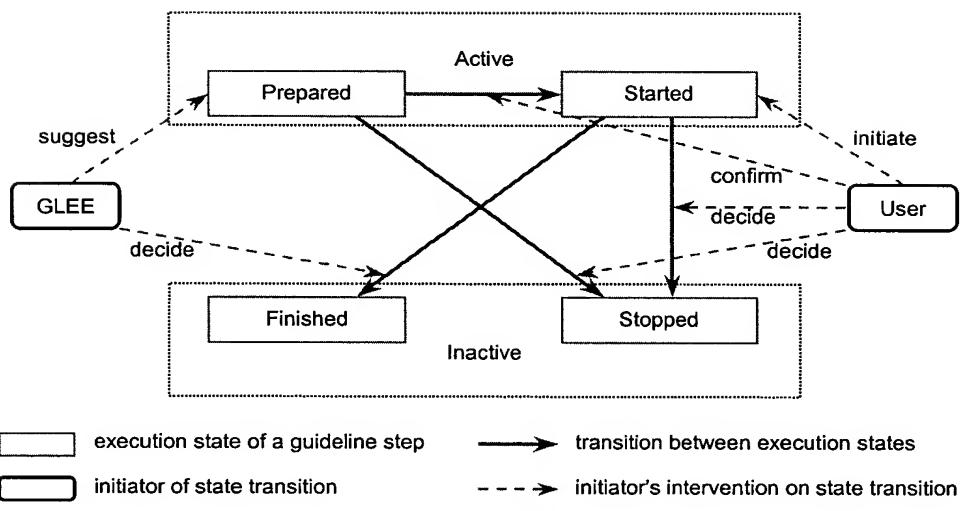


Fig. 3

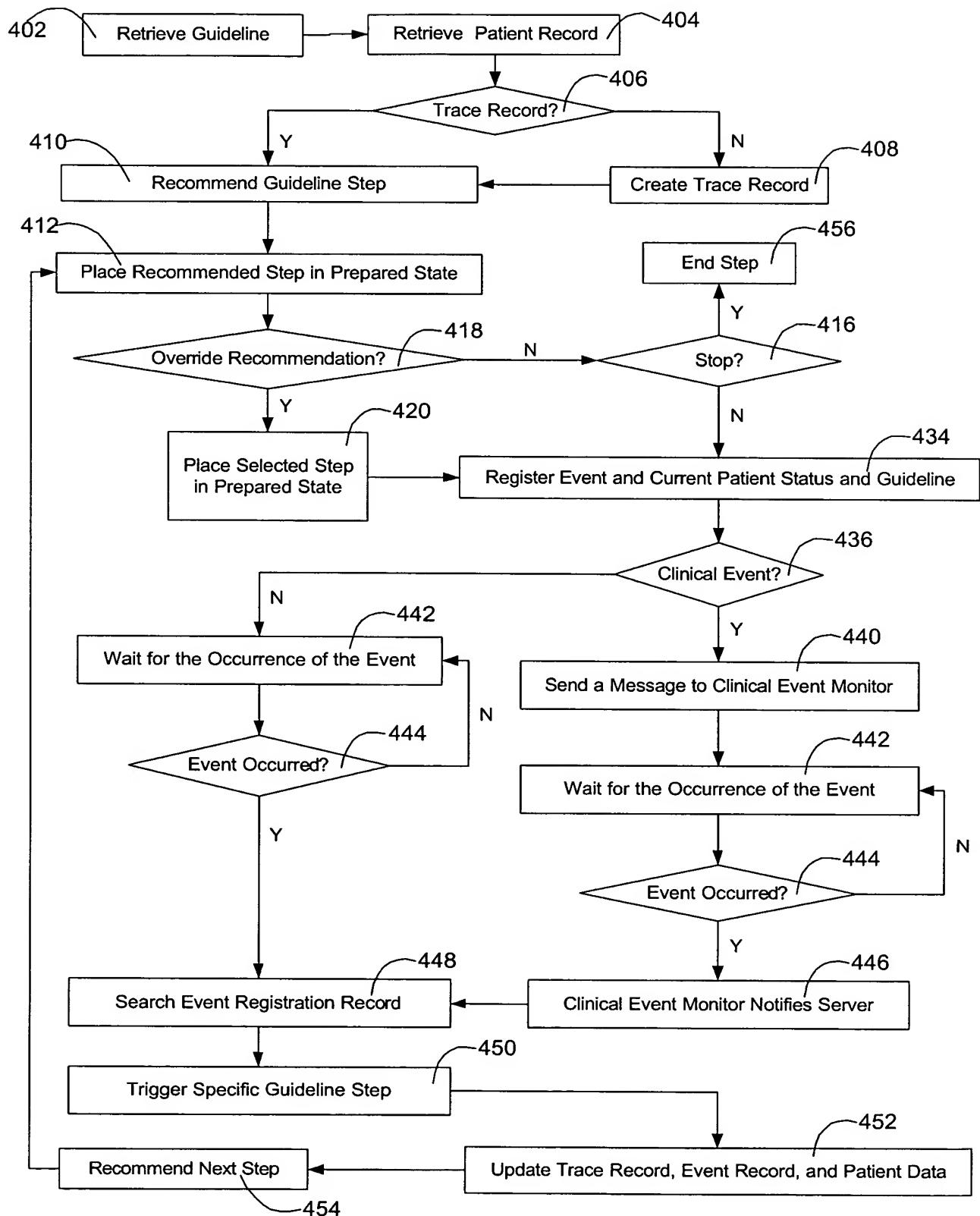


Fig. 4

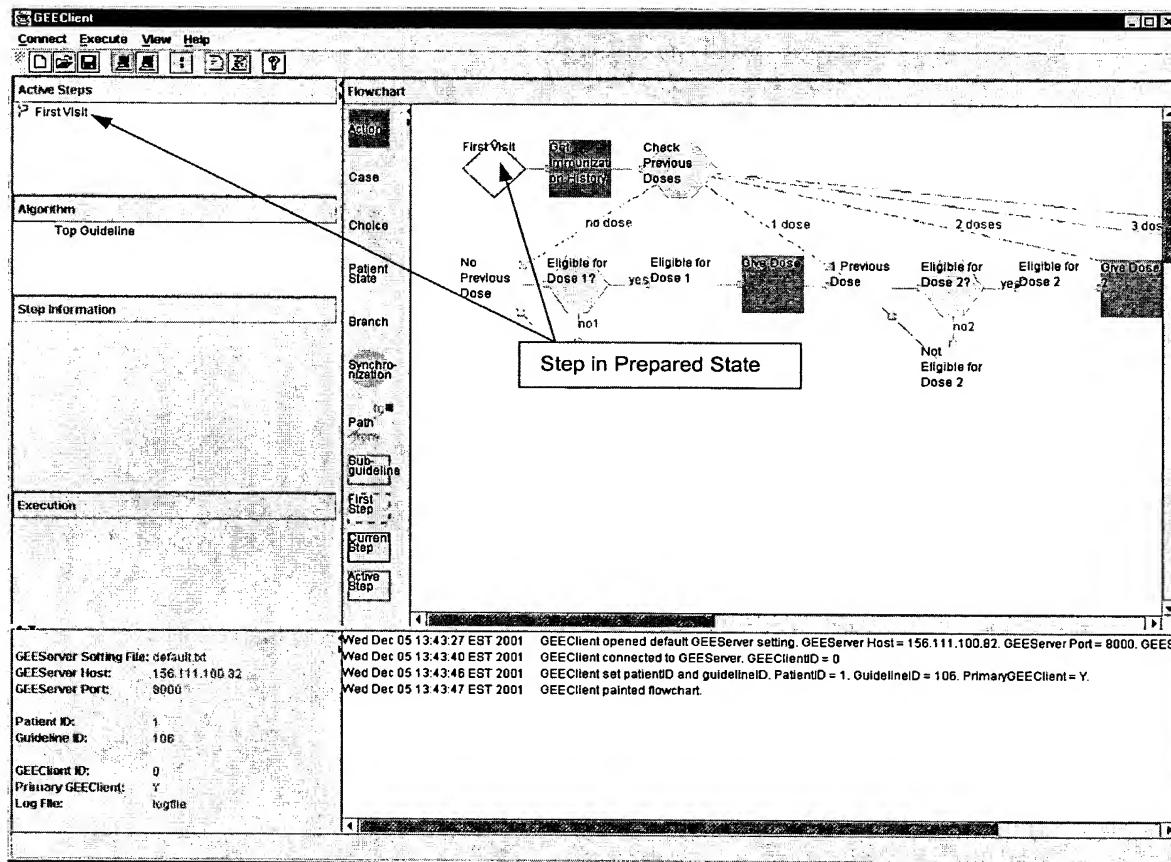


Fig. 5

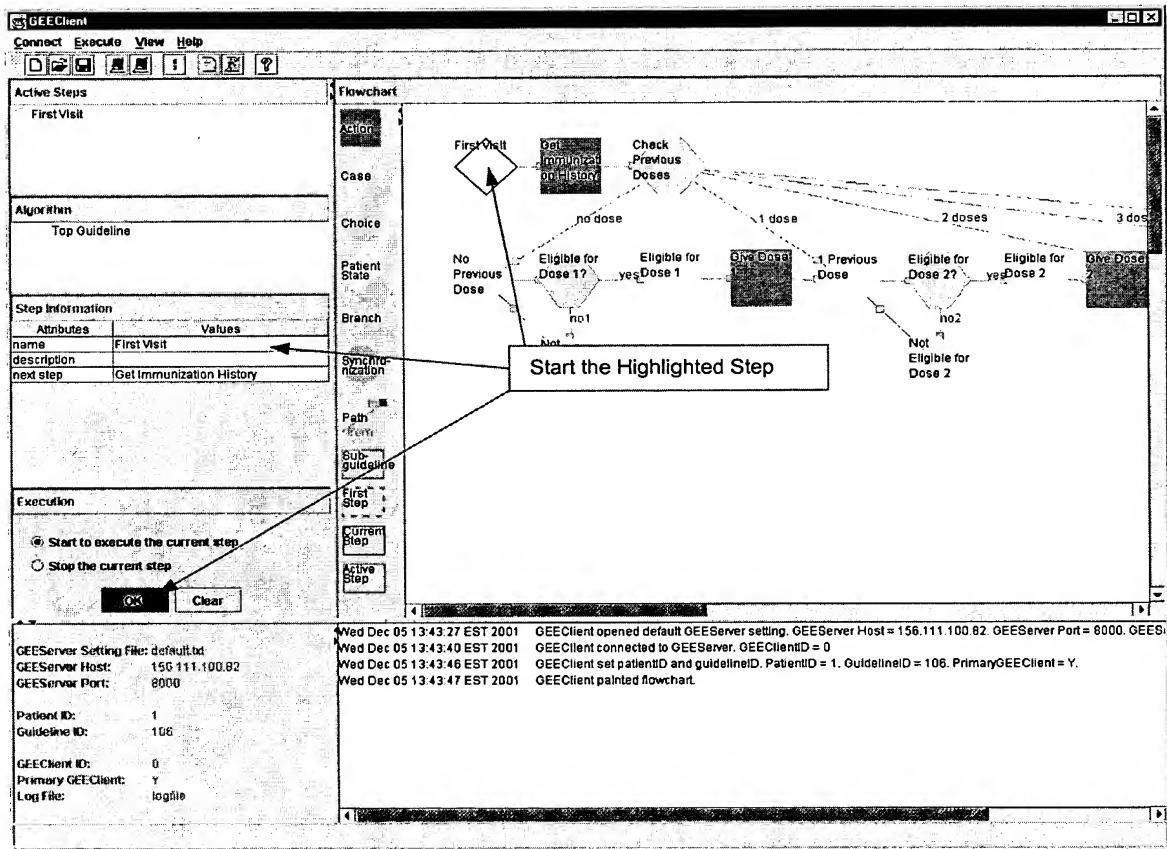


Fig. 6

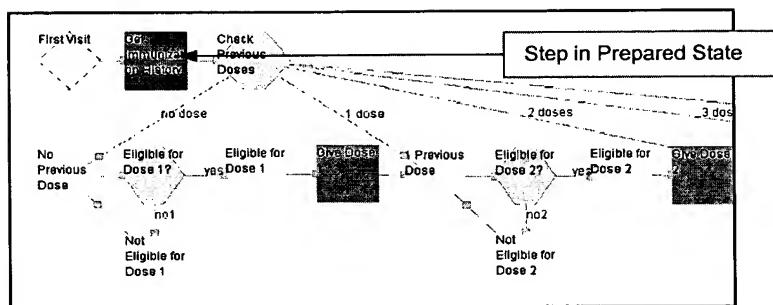


Fig. 7

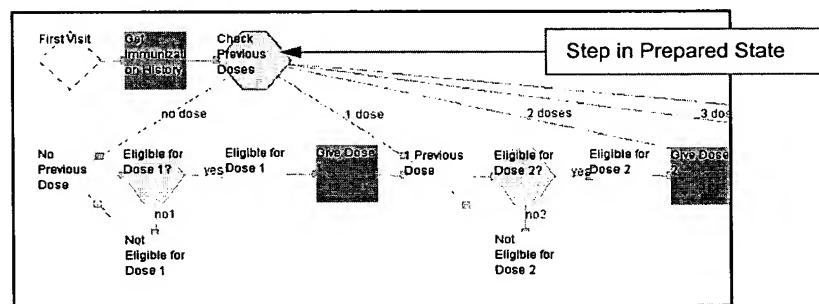


Fig. 8

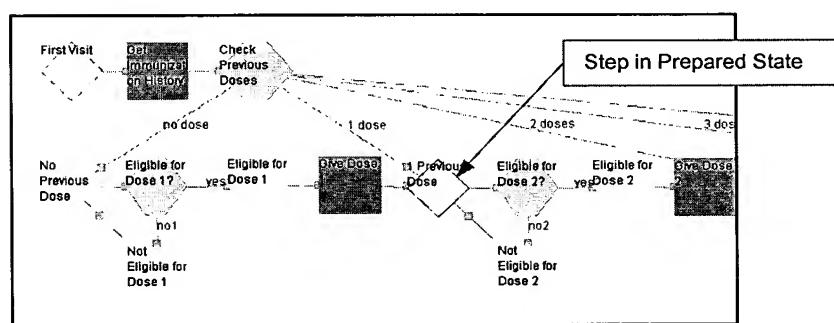


Fig. 9

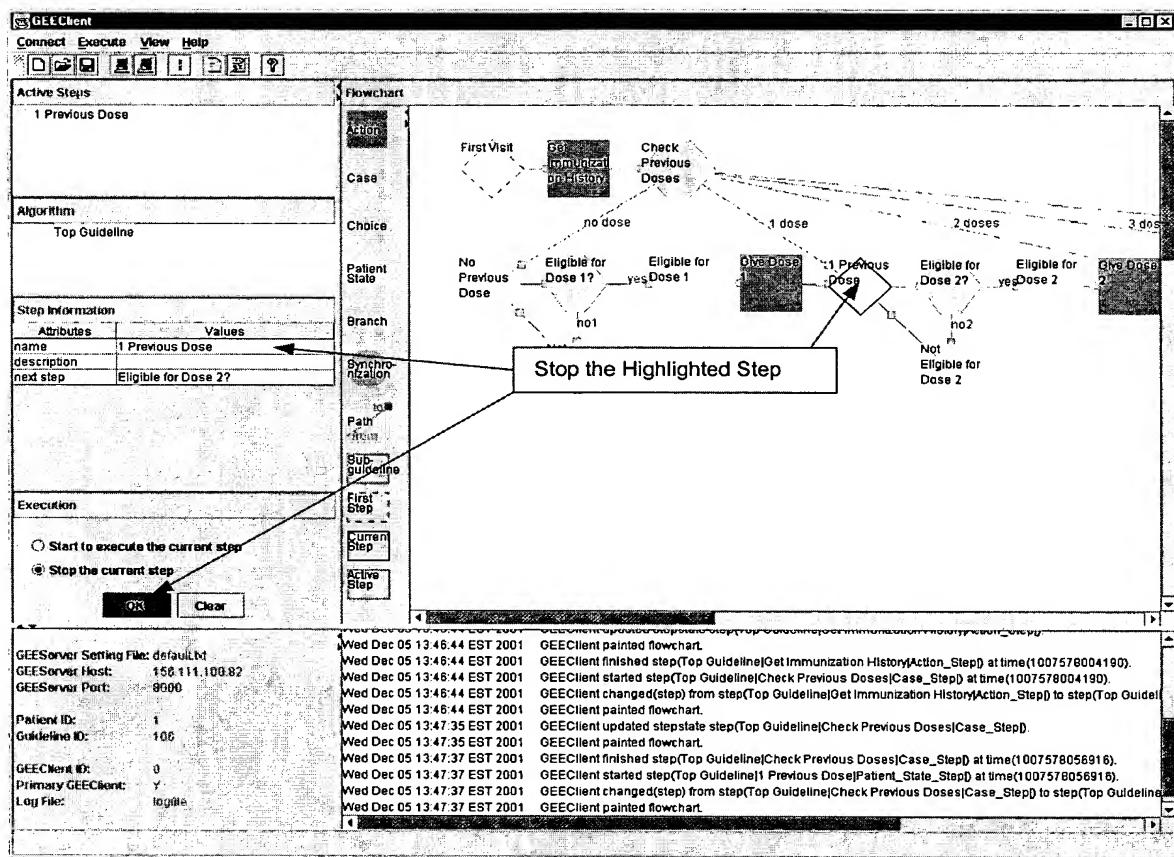


Fig. 10

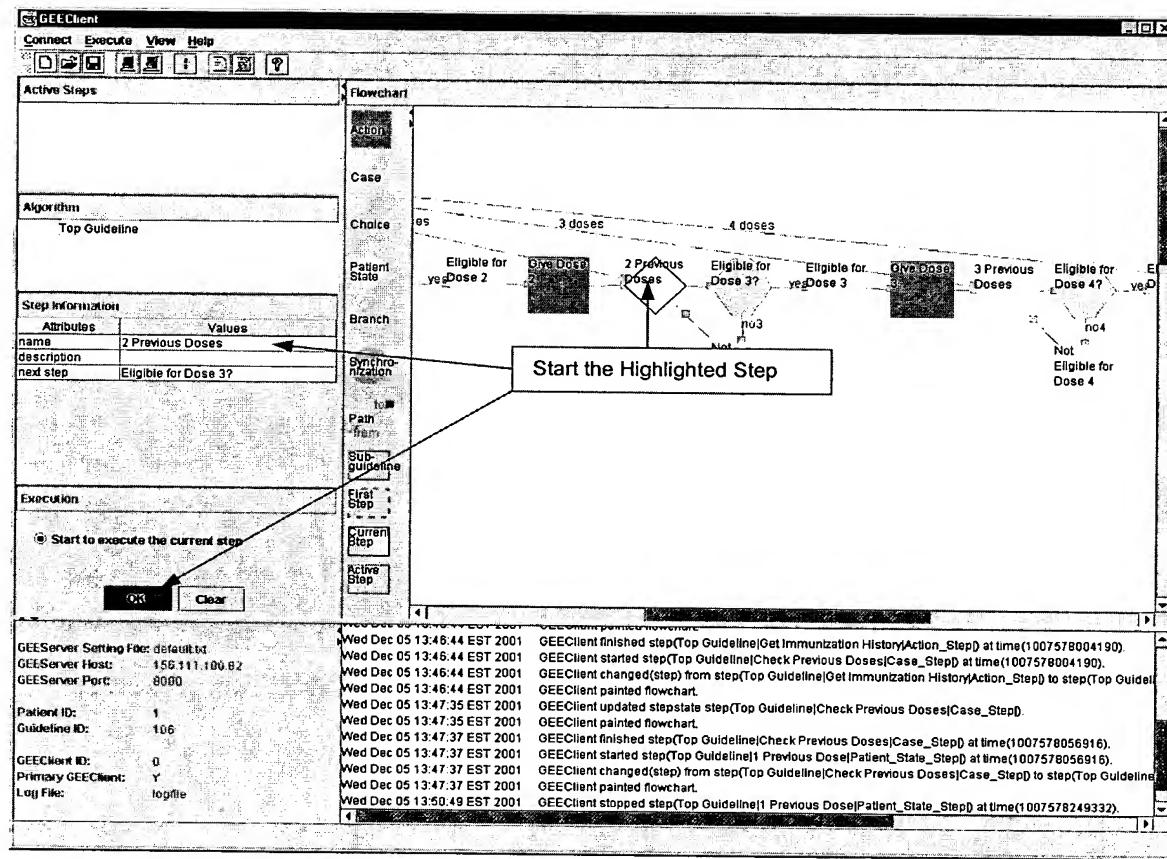


Fig. 11

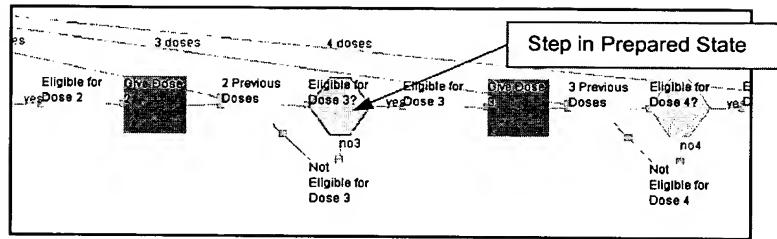


Fig. 12

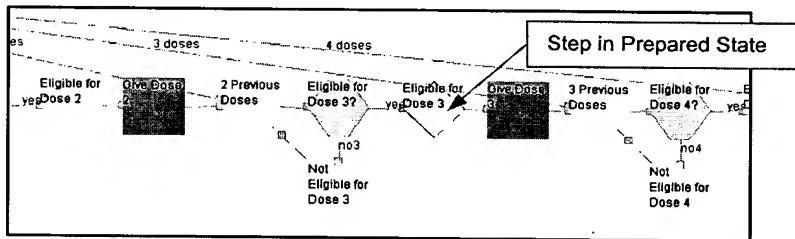


Fig. 13

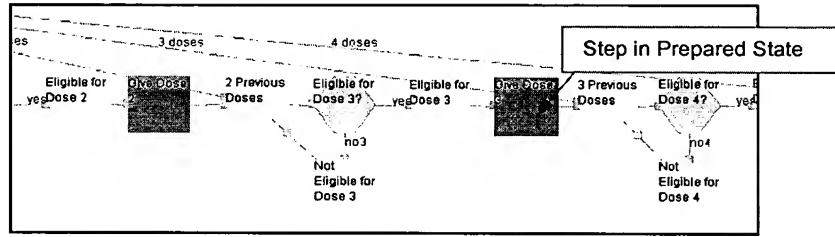


Fig. 14

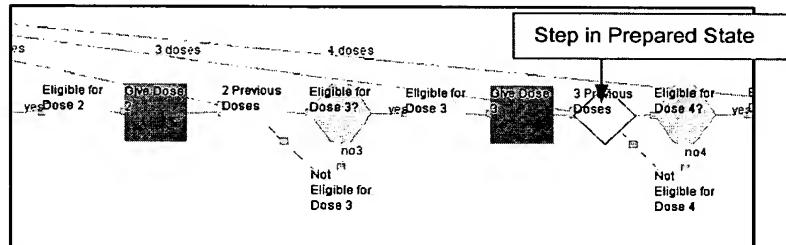


Fig. 15

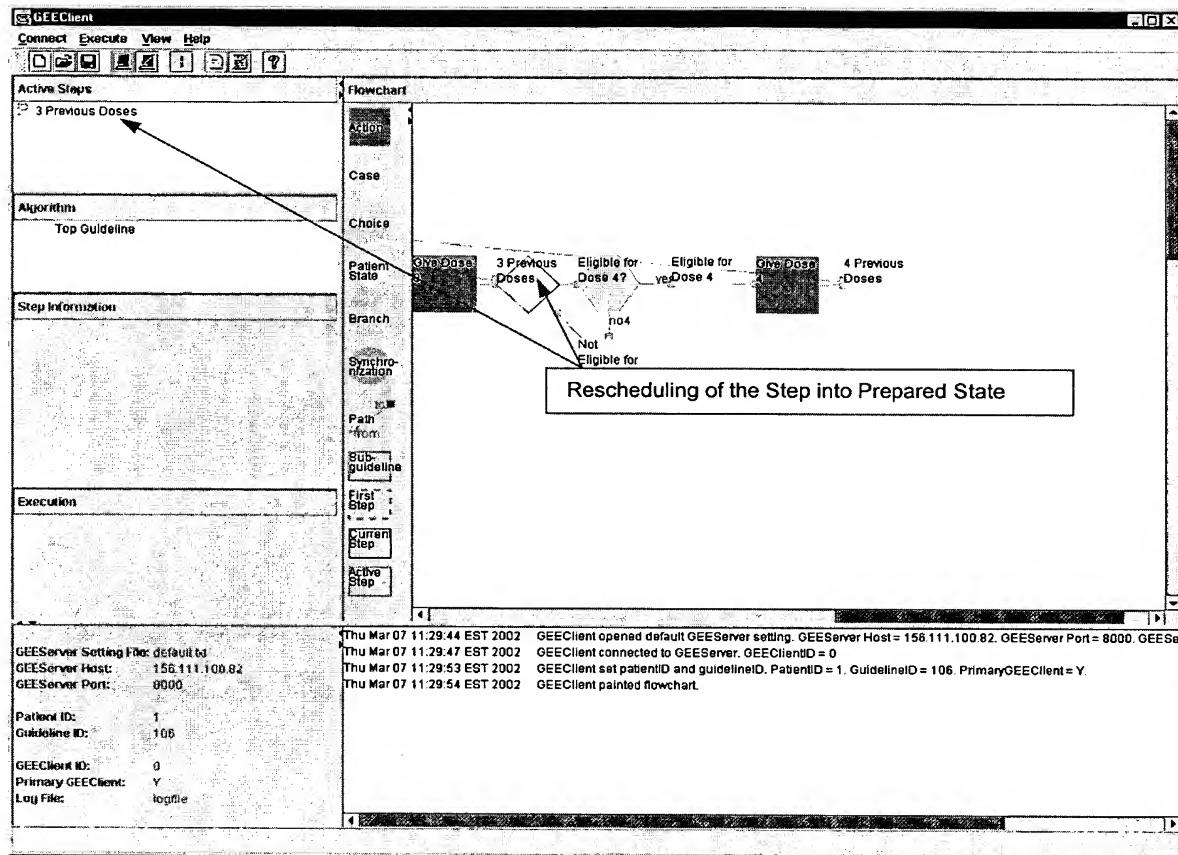


Fig. 16

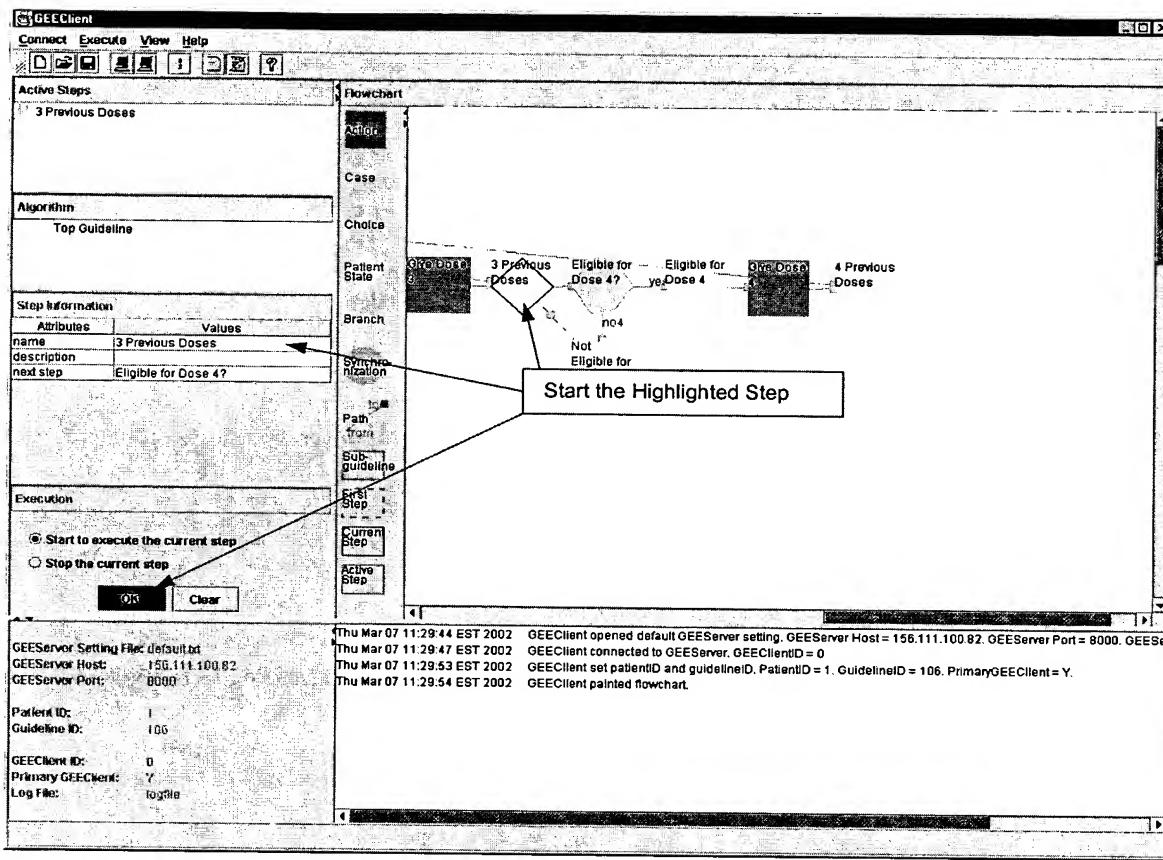


Fig. 17

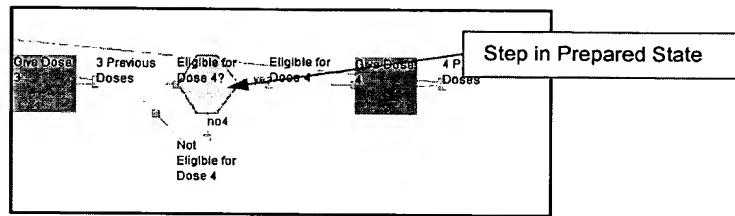


Fig. 18

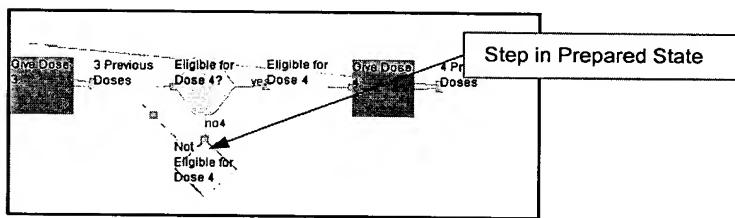


Fig. 19

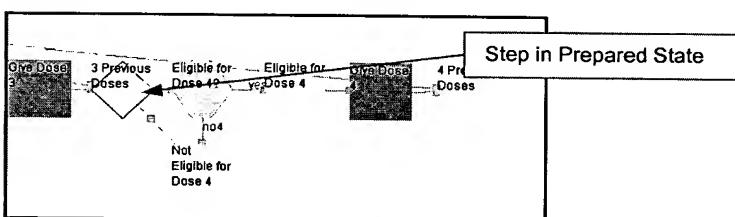


Fig. 20

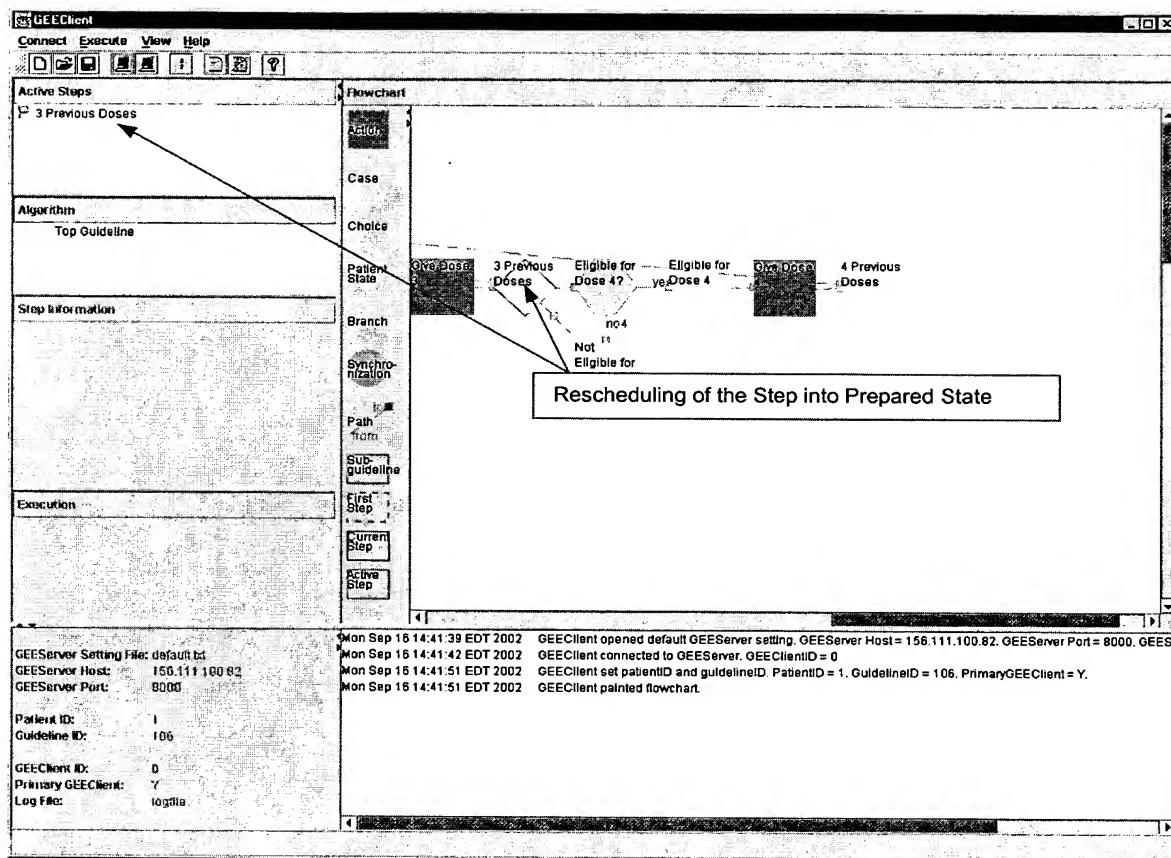


Fig. 21

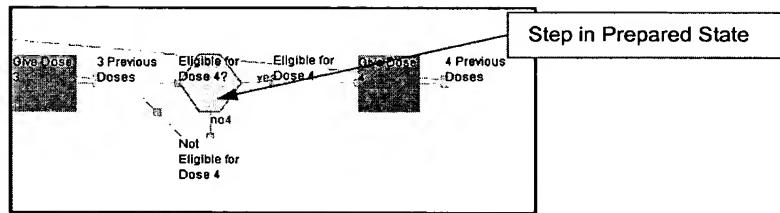


Fig. 22

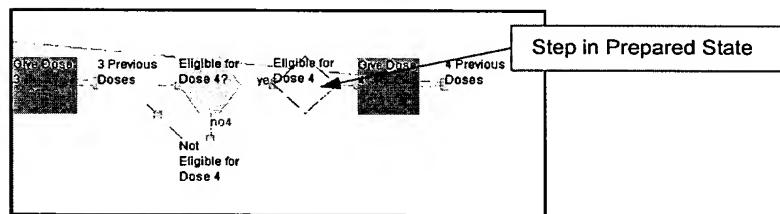


Fig. 23

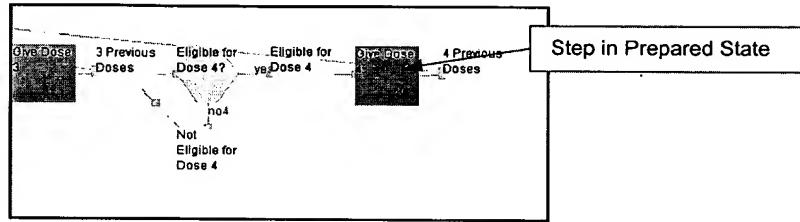


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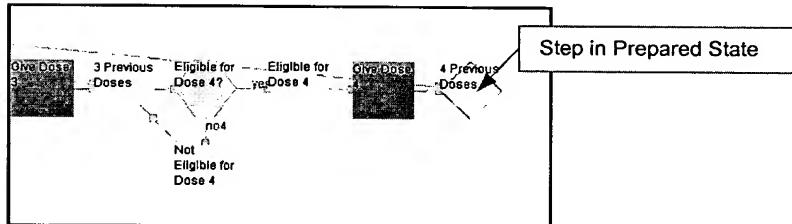


Fig. 25

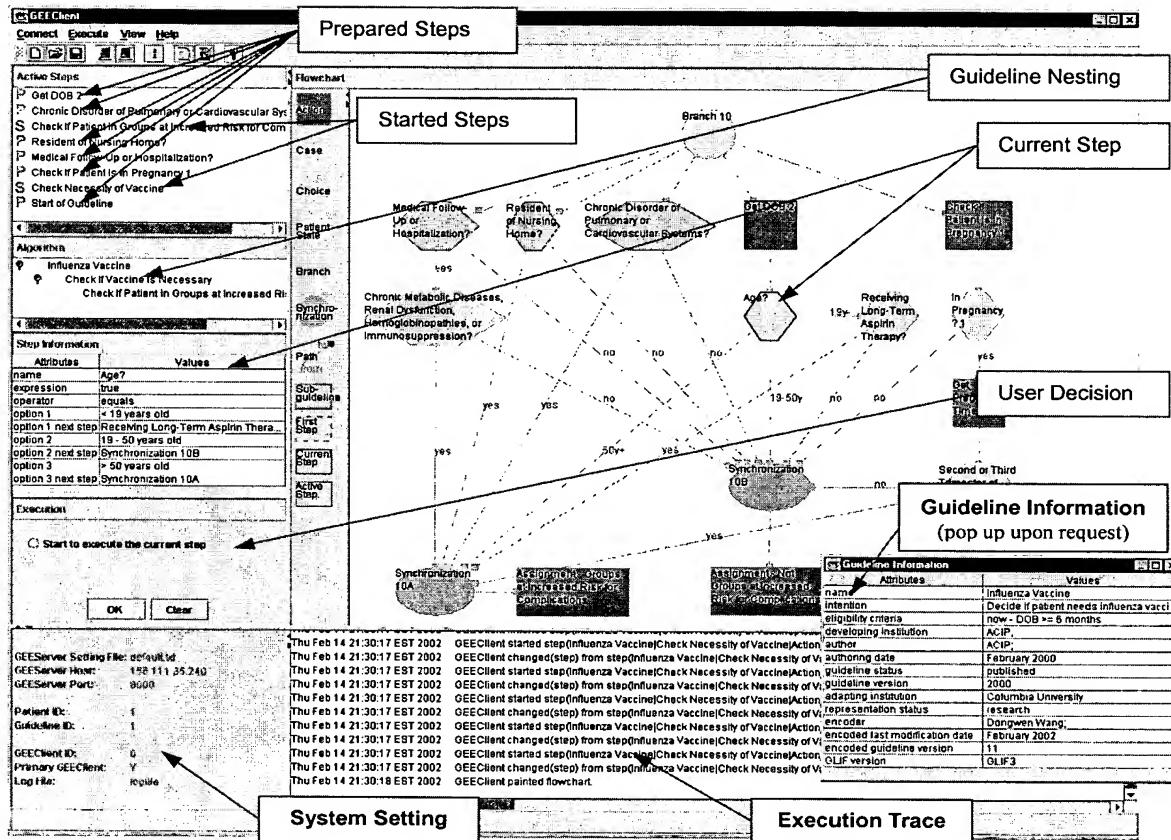


Fig. 26

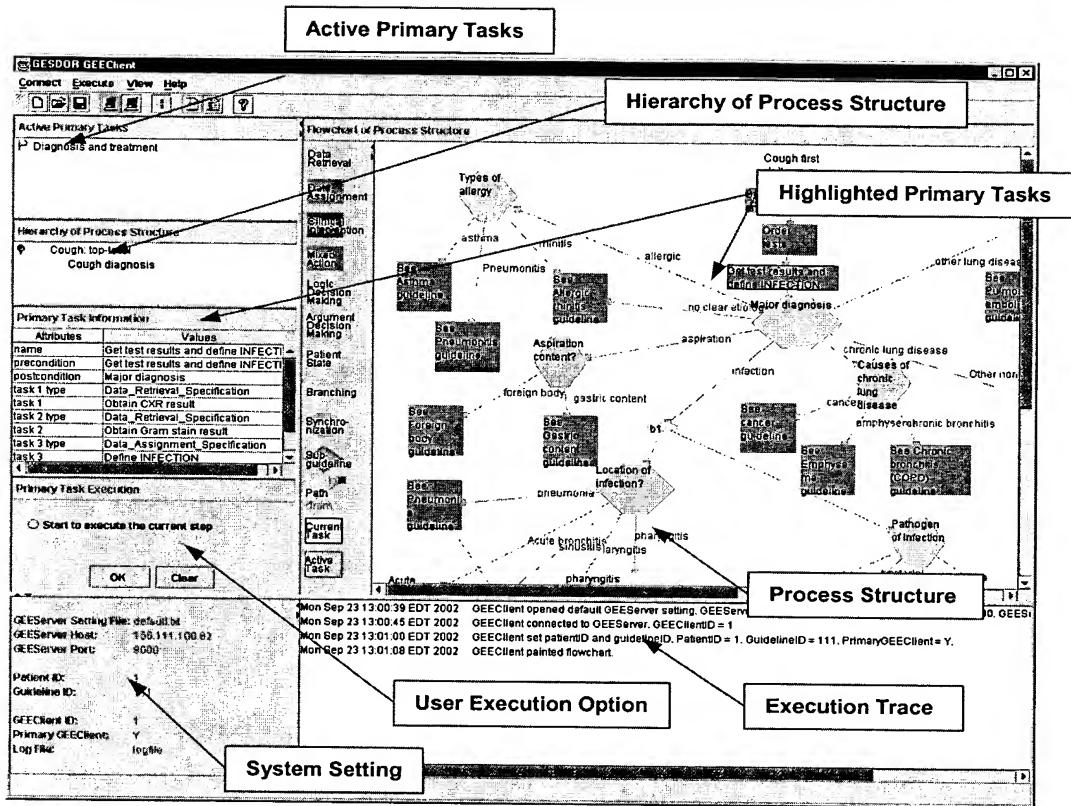


Fig. 27

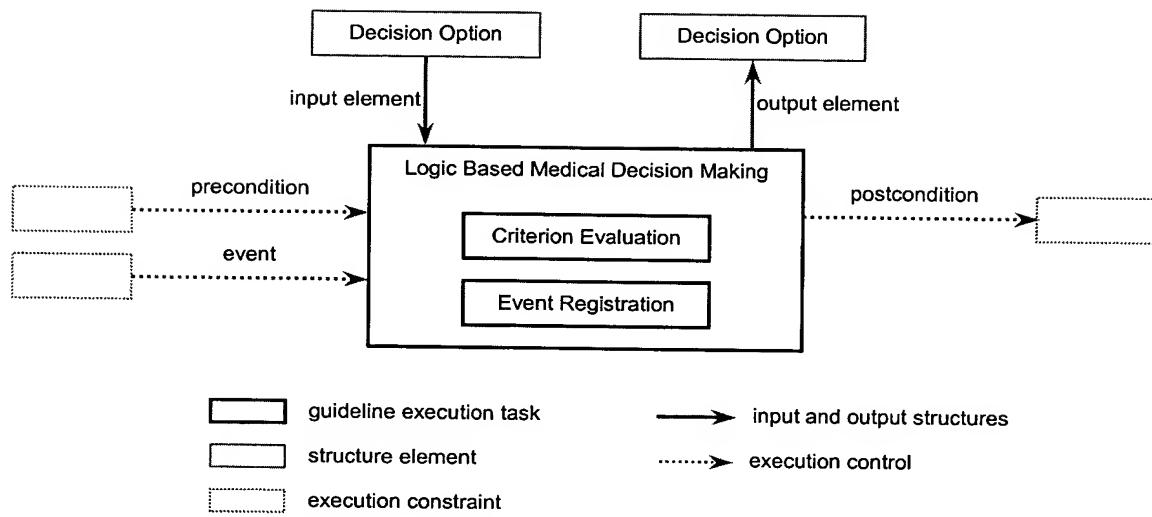


Fig. 28

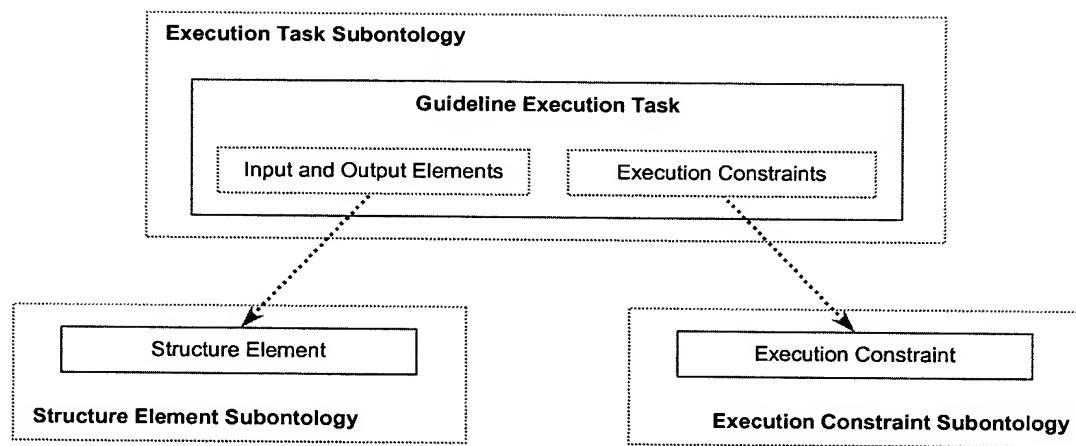


Fig. 29

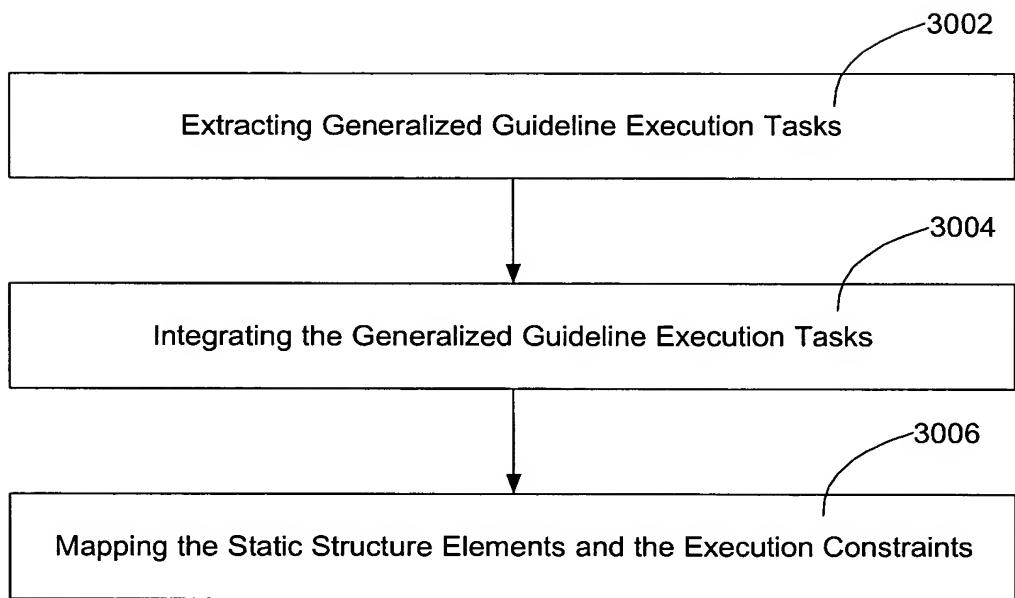


Fig. 30

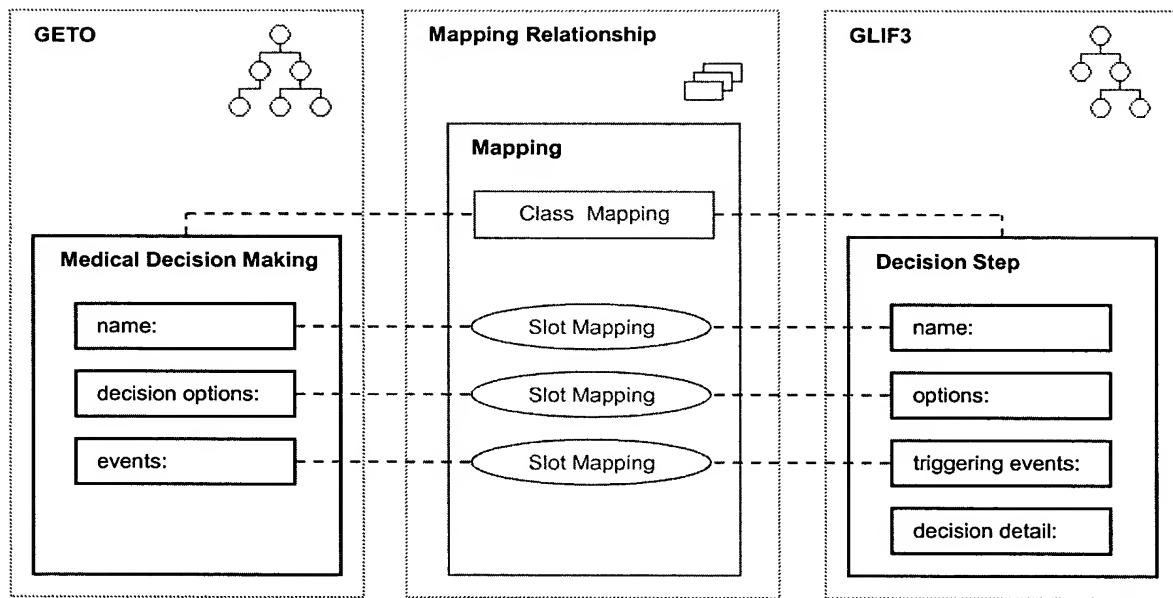
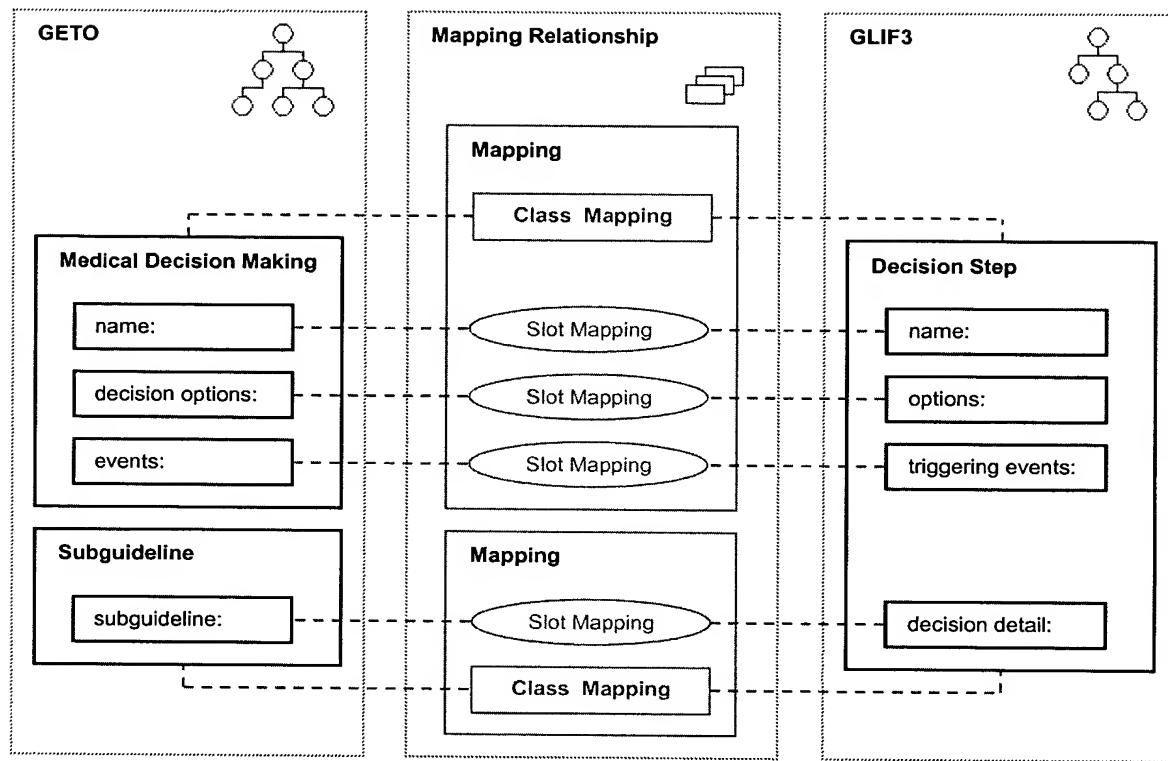


Fig. 31



	class		mapping relationship
	slot		class mapping
	slot mapping		

Fig. 32

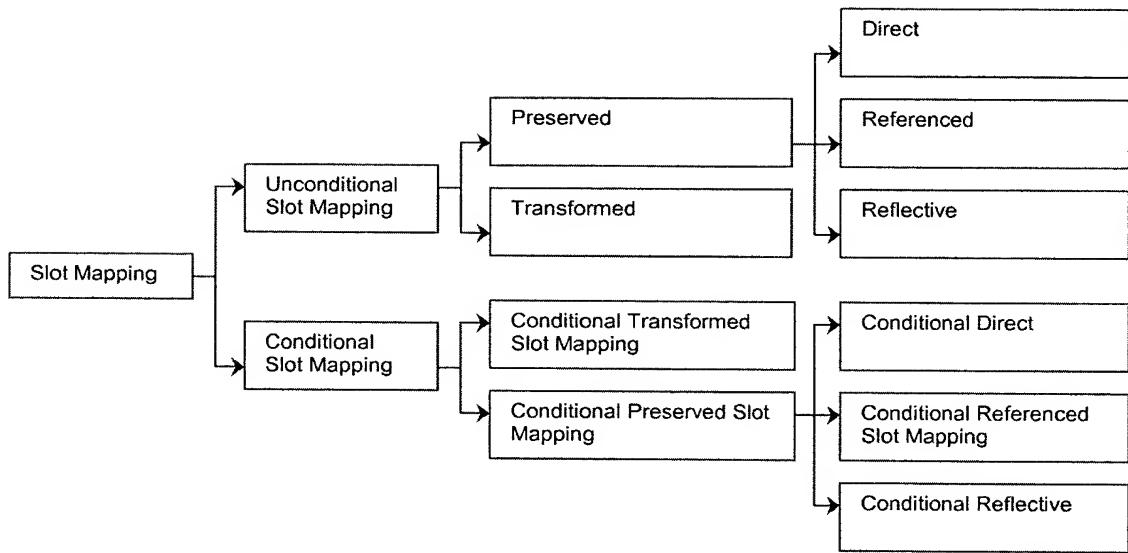


Fig. 33

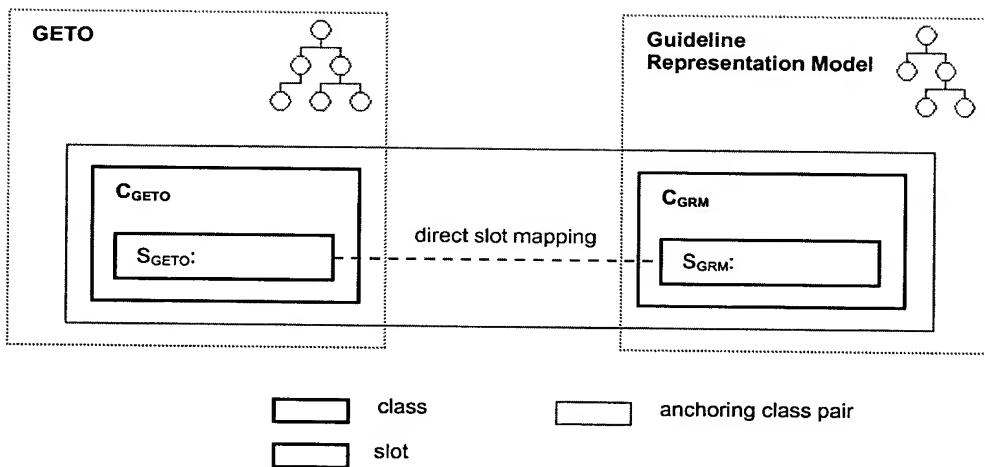


Fig. 34

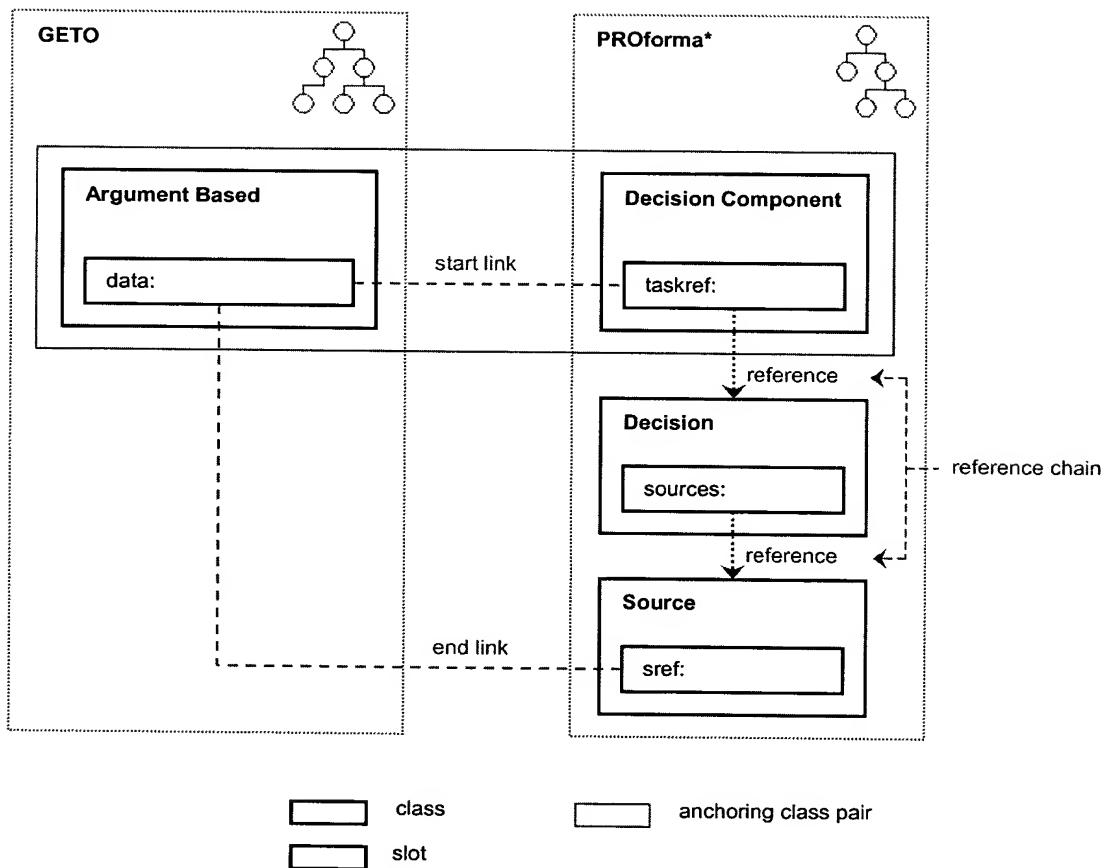


Fig. 35

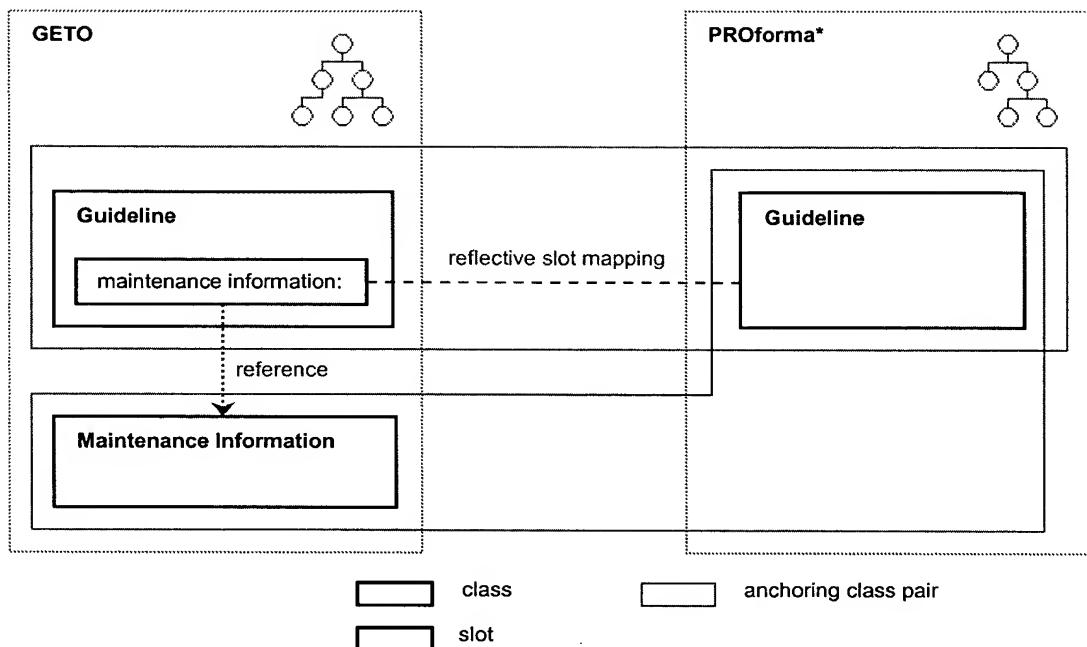


Fig. 36

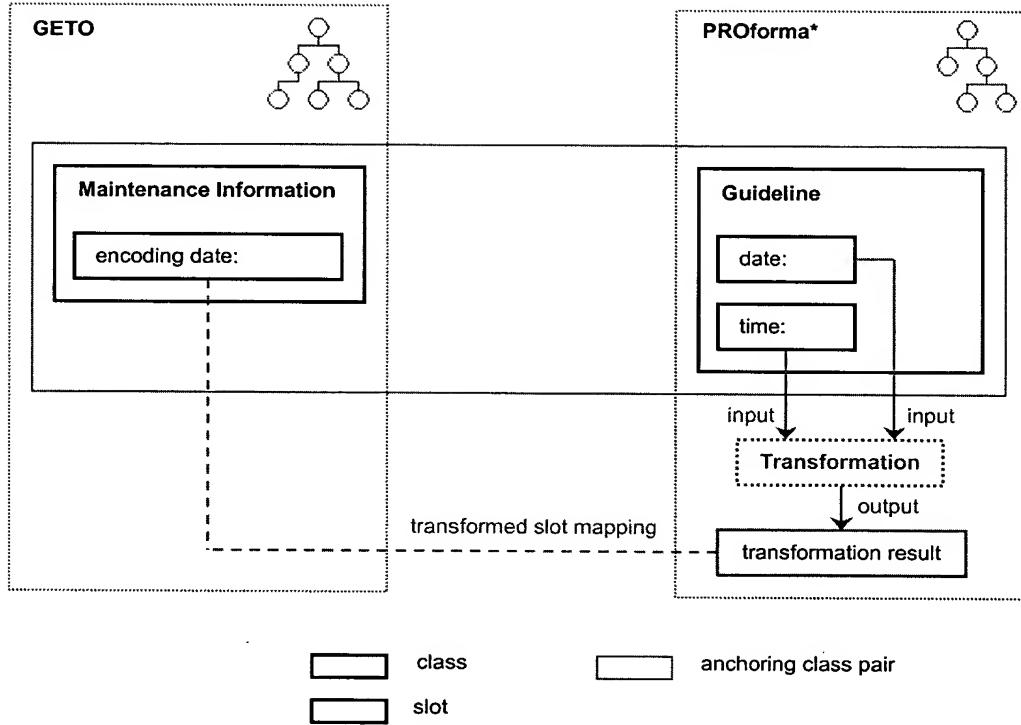


Fig. 37

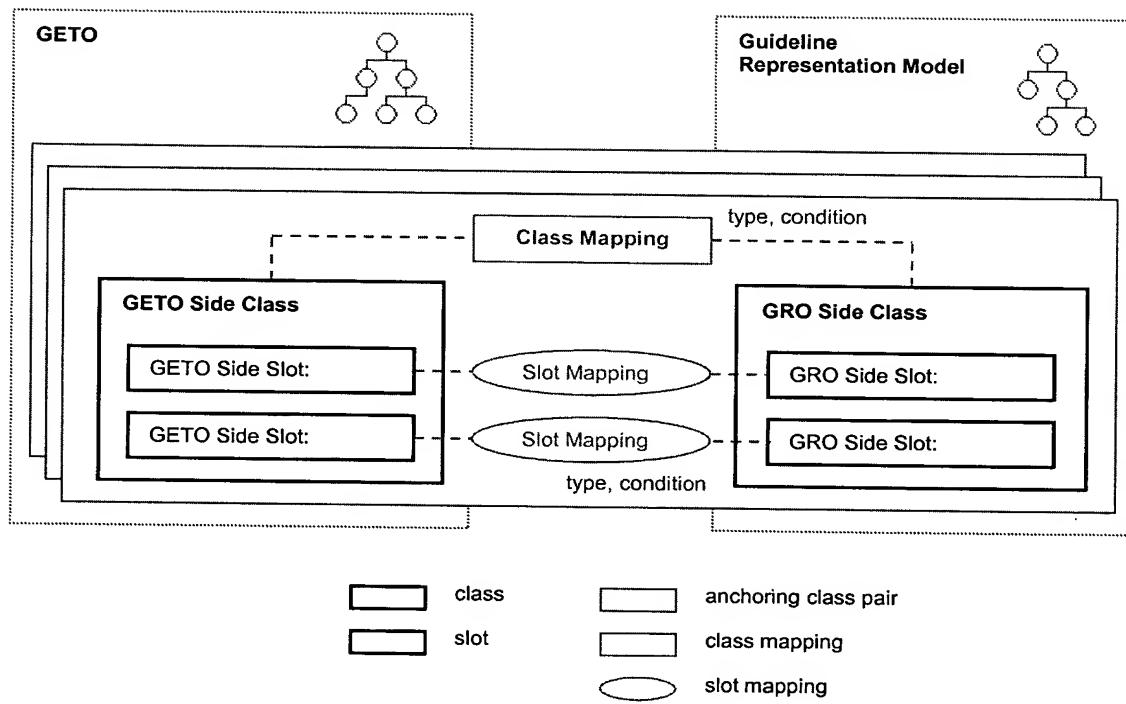


Fig. 38

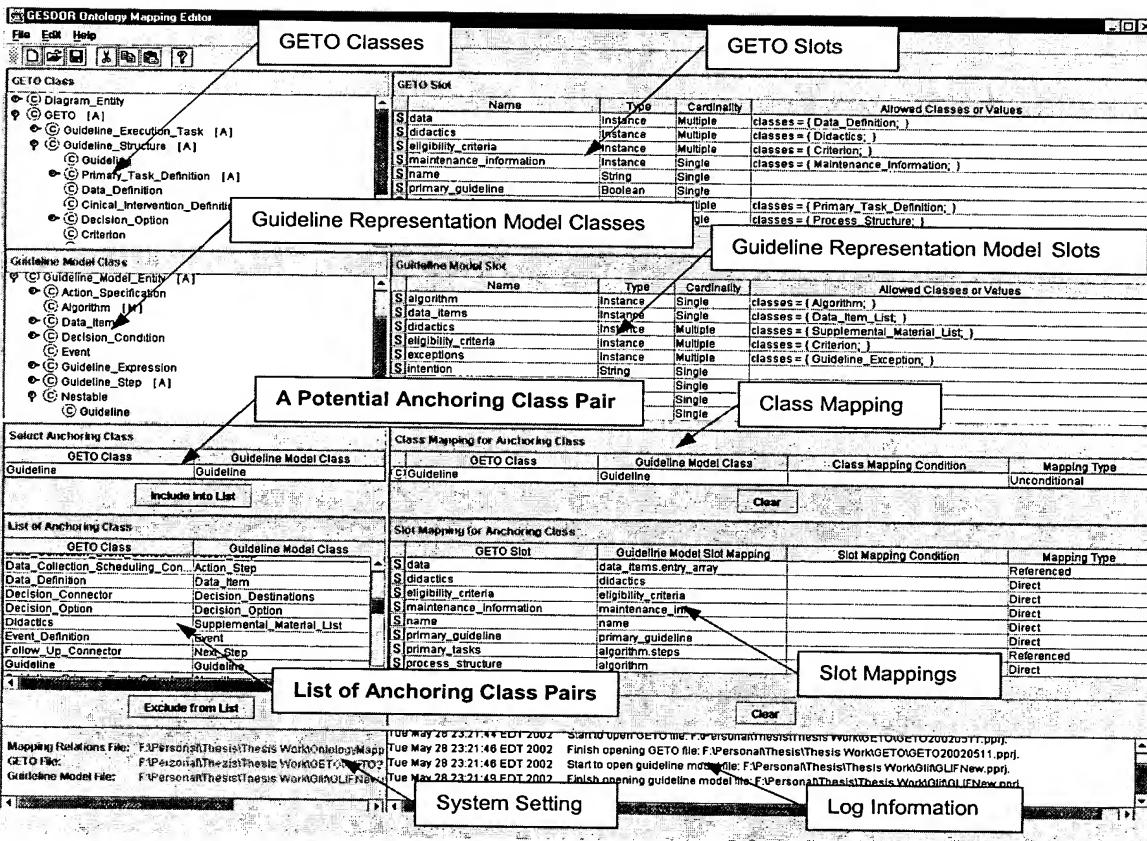


Fig. 39

Overview of the GESDOR Model

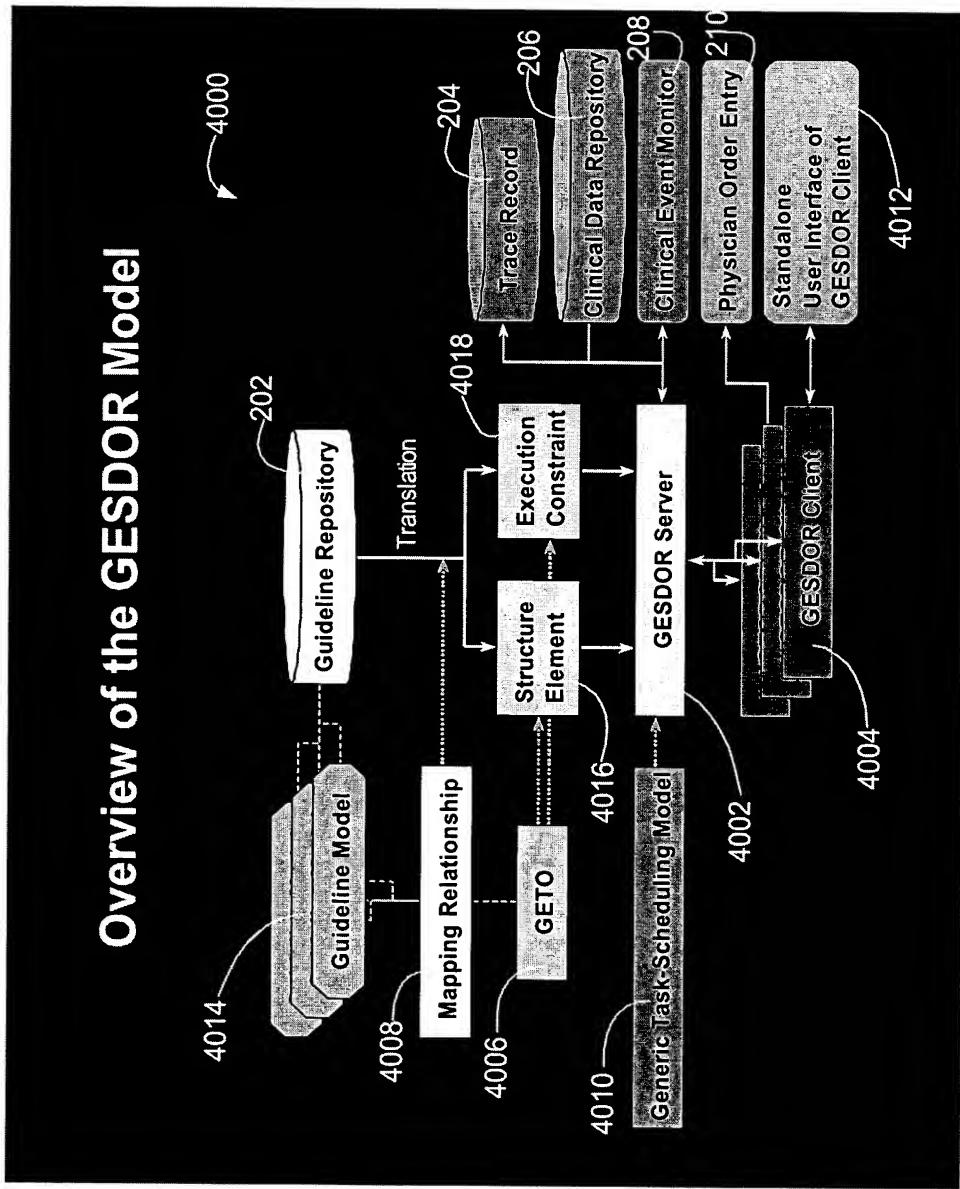


Fig. 40

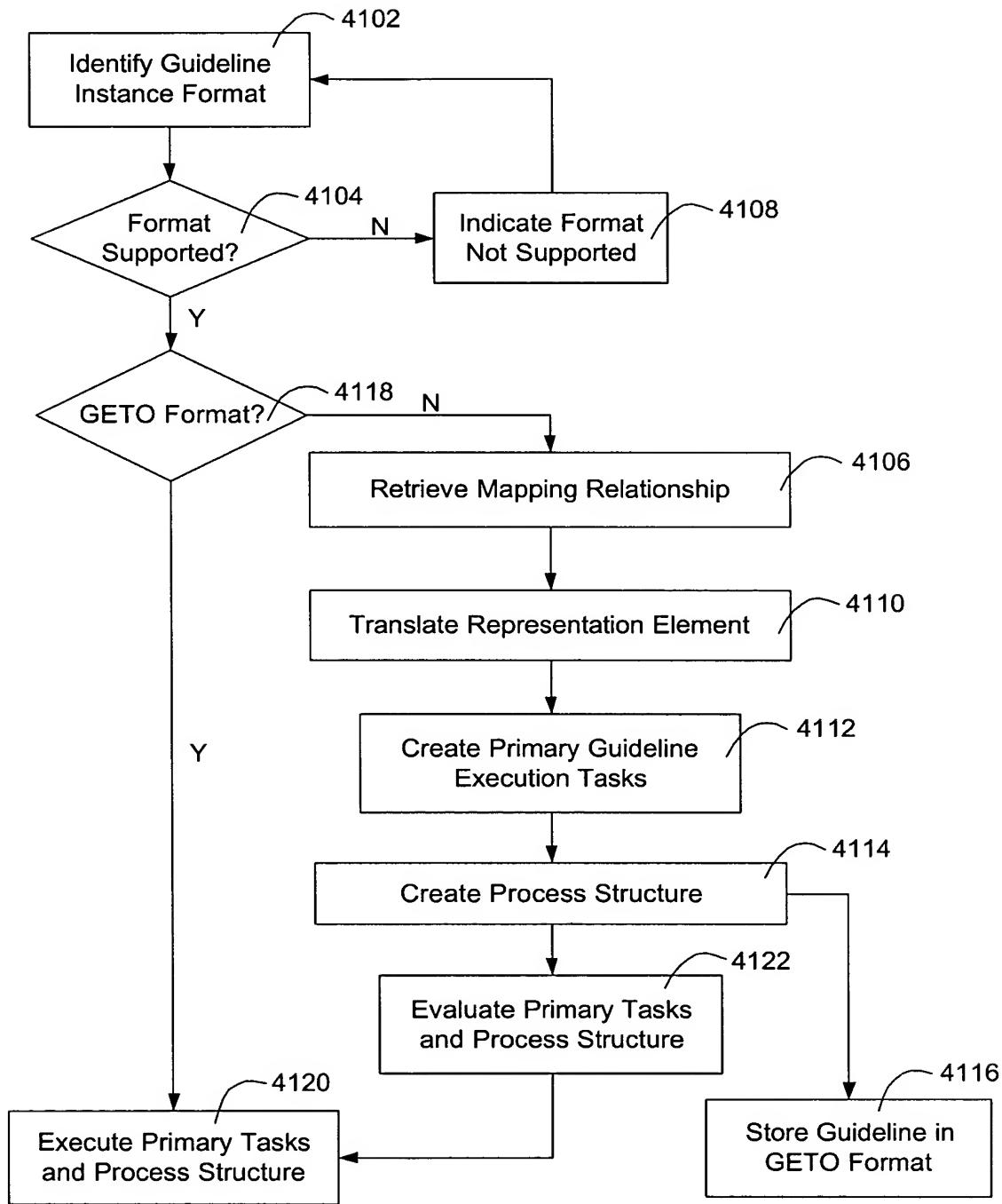


Fig. 41

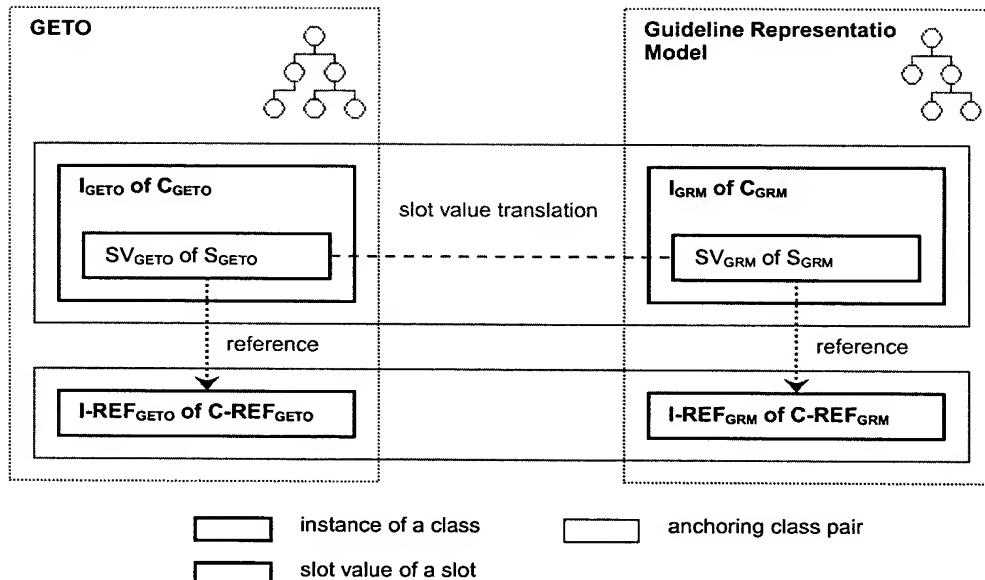


Fig. 42

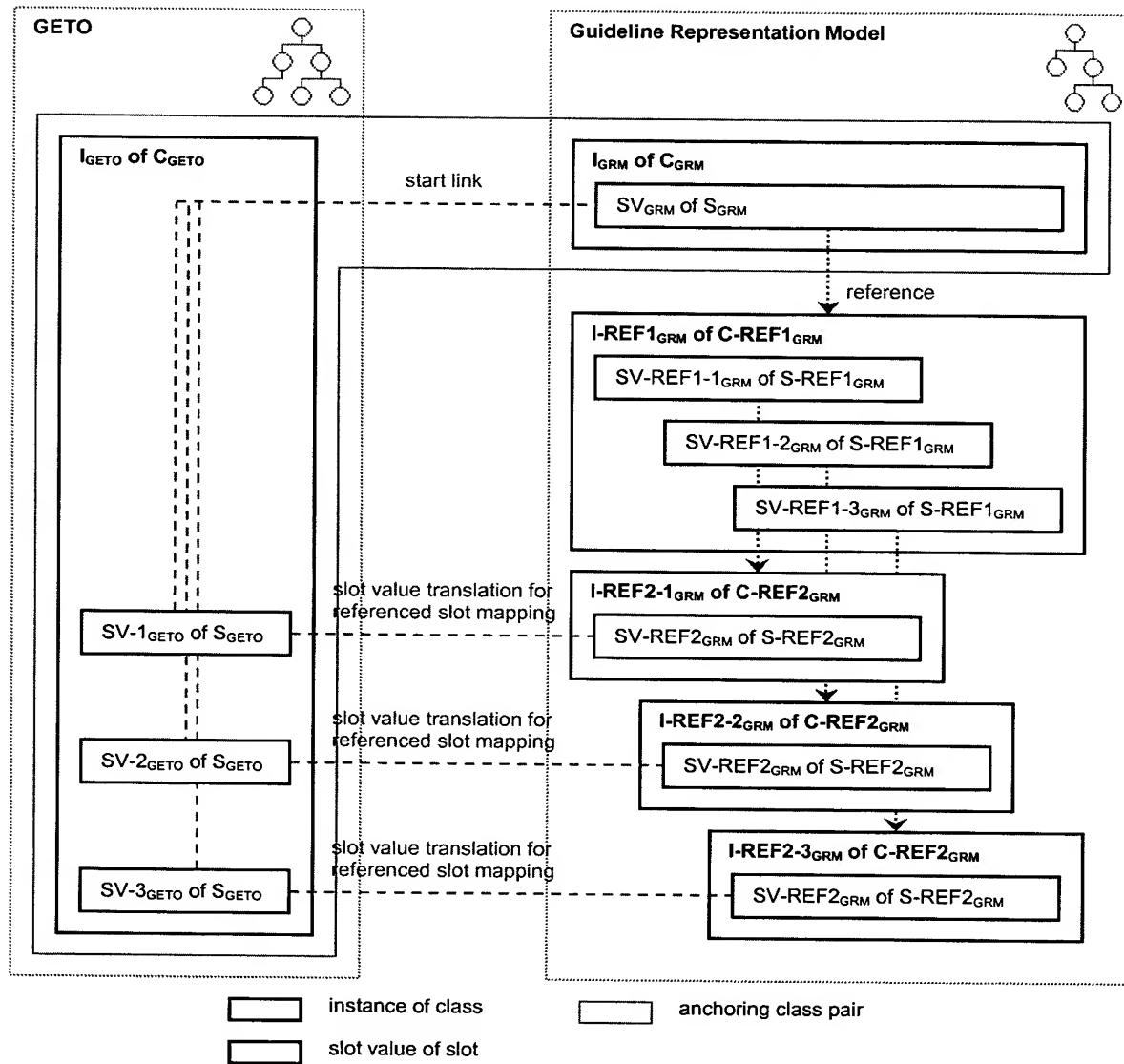


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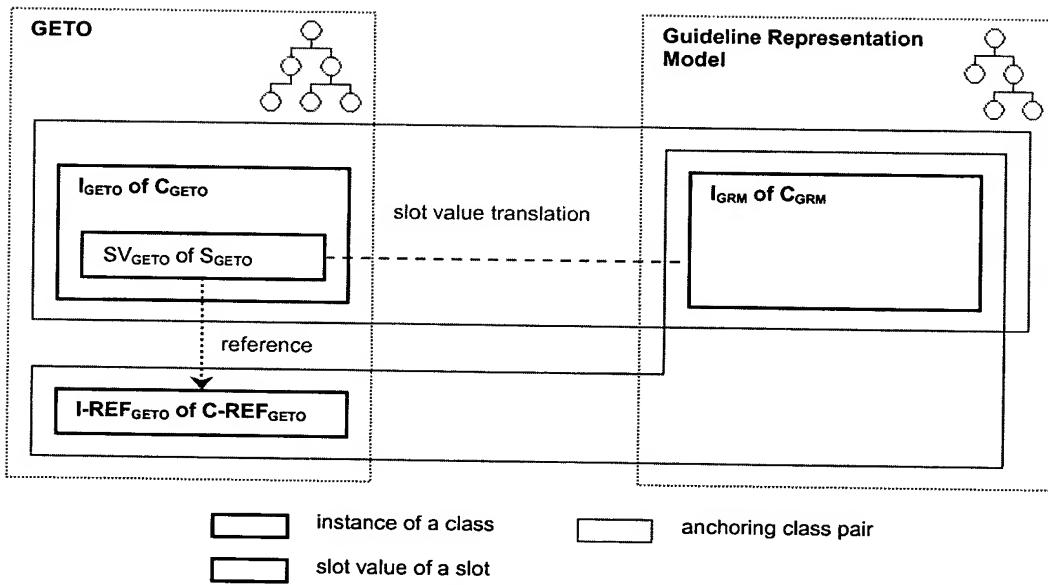


Fig. 44

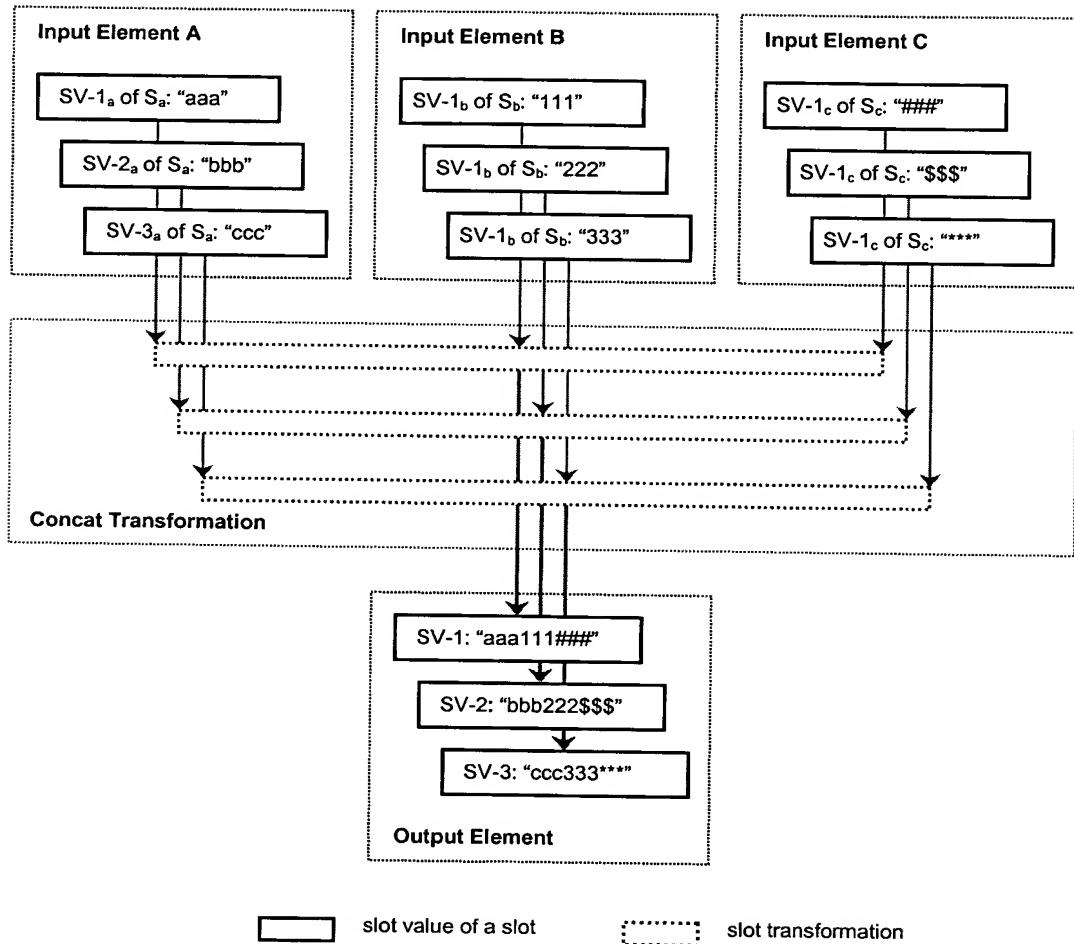


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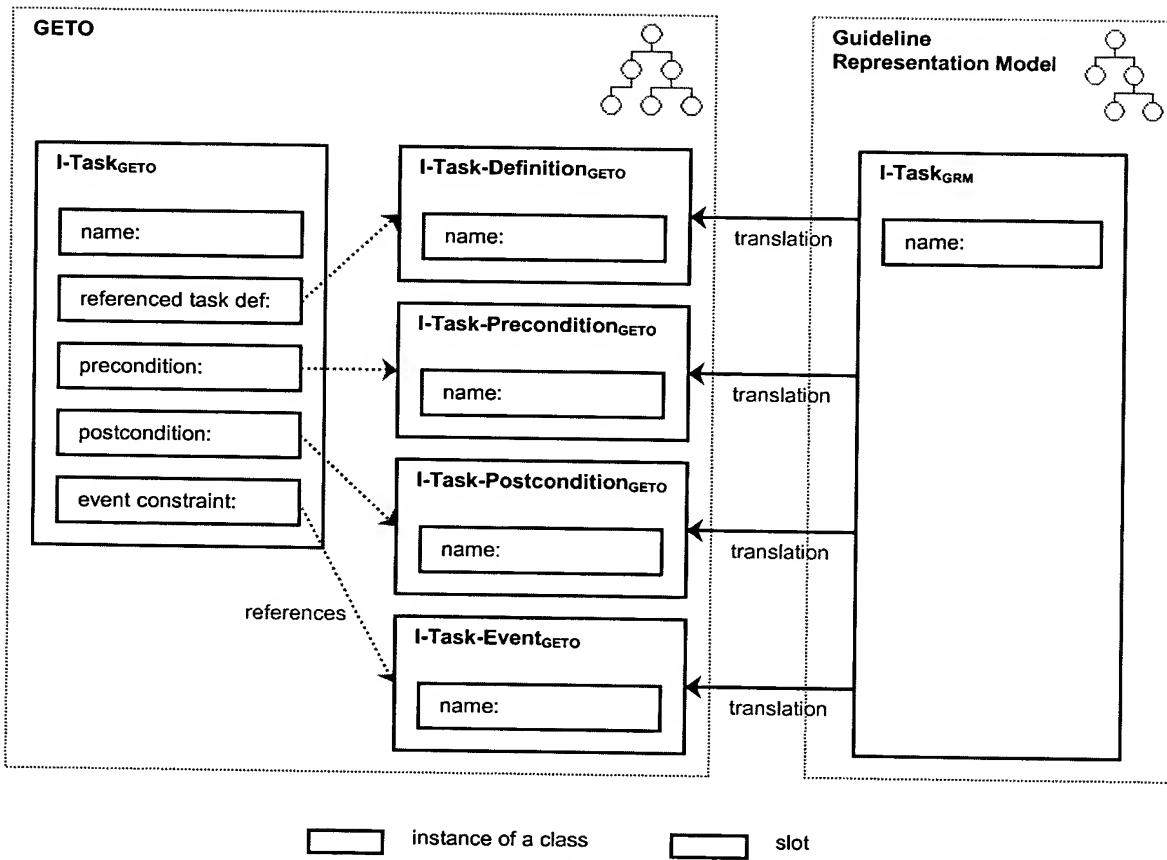
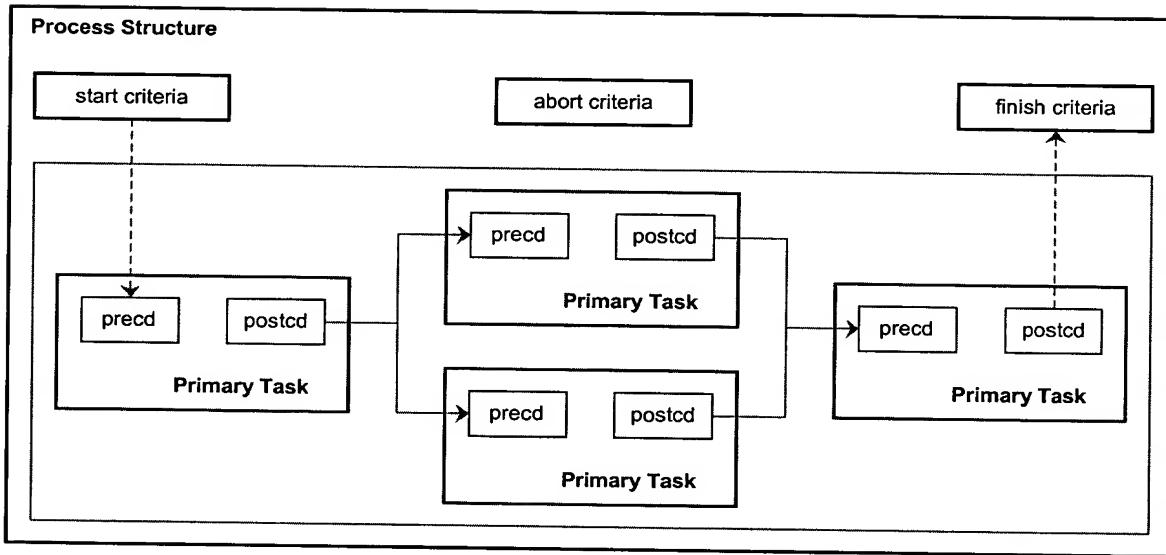


Fig. 46



--→ chaining between process structure and primary task

→ chaining between primary tasks

precd: precondition

postcd: postcondition

Fig. 47

Fig. 48

